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## NTE5726 Powerblock Module

**Description:**

The NTE5726 uses high voltage power thyristors/diodes and is electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. This device is intended for general purpose applications such as battery chargers, welders and plating equipment and where high voltage and high current are required.

**Features:**

- High Voltage
- Electrically Isolated Base Plate
- 3000V<sub>RMS</sub> Isolating Voltage
- High Surge Capability
- Large Creepage Distances

**Ratings and Characteristics:**

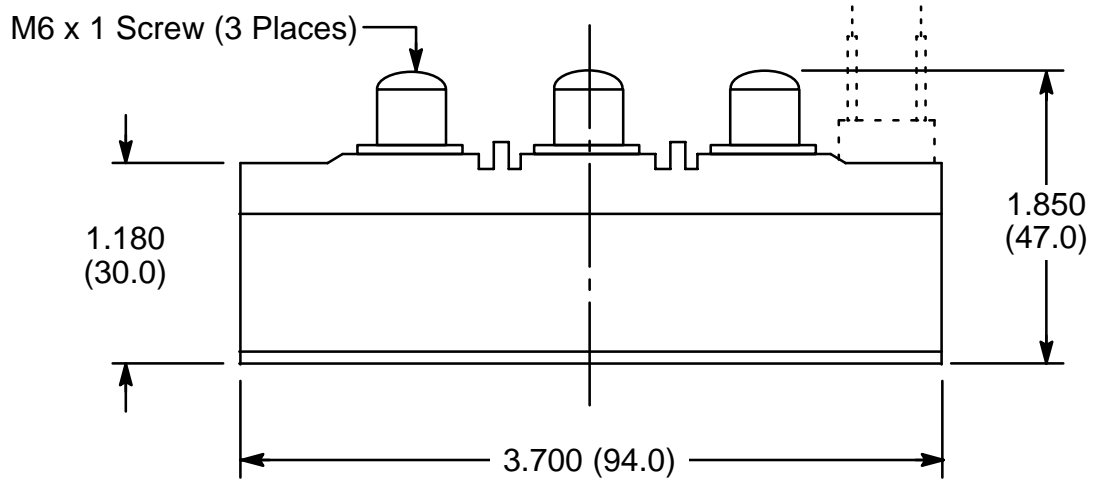
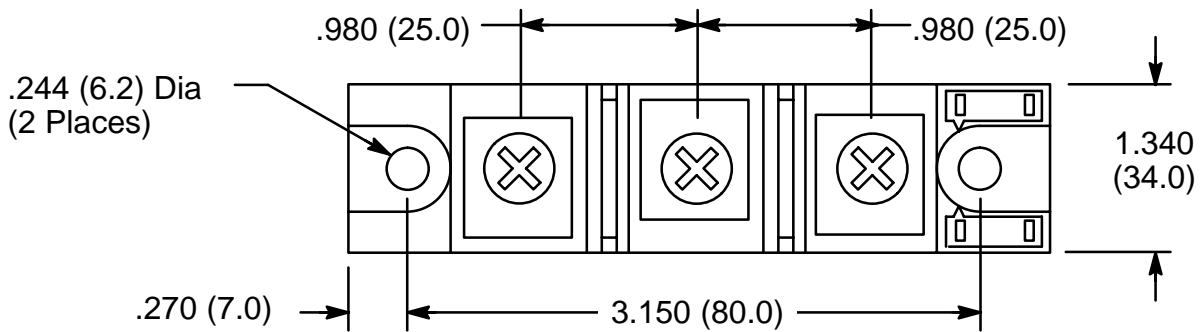
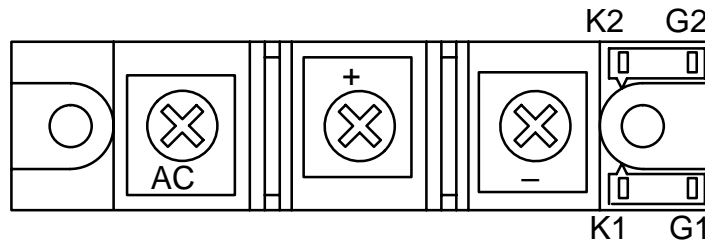
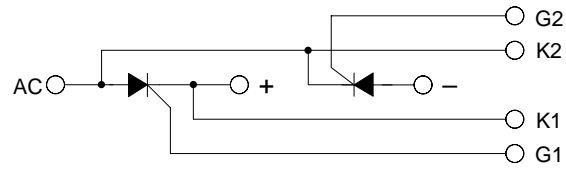
Average Forward Current ( $T_C = +85^\circ\text{C}$ , 180° Conduction, Half Sine Wave), $I_{F(AV)}$ .....	160A
Maximum RMS On-State Current (As AC Switch), $I_{T(RMS)}$ .....	355A
Maximum Repetitive Peak Reverse and Off-State Blocking Voltage, $V_{RRM}$ , $V_{DRM}$ .....	1600V
Maximum Non-Repetitive Peak Reverse Voltage, $V_{RSM}$ .....	1700V
Maximum Peak Reverse and Off-State Leakage Current ( $T_J = +125^\circ\text{C}$ ), $I_{RRM}$ , $I_{DRM}$ .....	50mA
RMS Isolation Voltage (50Hz, Circuit to Base, All Terminals Shorted, $t = 1\text{s}$ ), $V_{ISO}$ .....	3000V
Critical Rate of Rise of Off-State Voltage ( $T_J = +125^\circ\text{C}$ ), $dv/dt$	
(Linear to 80% Rated $V_{DRM}$ ) .....	500V/ $\mu\text{s}$
(Linear to 67% Rated $V_{DRM}$ ) .....	1000V/ $\mu\text{s}$
Operating Junction Temperature Range, $T_J$ .....	-40° to +125°C
Storage Temperature Range, $T_{stg}$ .....	-40° to +150°C
Thermal Resistance, Junction-to-Case (Per Junction, DC Operation), $R_{thJC}$ .....	0.170°C/W
Thermal Resistance, Case-to-Sink (Per Module, Note 1), $R_{thCS}$ .....	0.05°C/W

Note 1. Mounting surface flat, smooth and greased.

## Electrical Specifications:

Parameter	Symbol	Test Conditions		Rating	Unit
Maximum Peak One-Cycle Non-Repetitive Surge Current	$I_{FSM}$	t = 10ms	Sinusoidal Half Wave, 100% $V_{RRM}$ Reapplied, Initial $T_J = +125^\circ\text{C}$	4300	A
		t = 8.3ms		4500	A
		t = 10ms	Sinusoidal Half Wave, No Voltage Reapplied, Initial $T_J = +125^\circ\text{C}$	5100	A
		t = 8.3ms		5350	A
Maximum $I^2t$ for Fusing	$I^2t$	t = 10ms	Sinusoidal Half Wave, 100% $V_{RRM}$ Reapplied, Initial $T_J = +125^\circ\text{C}$	92.5	$\text{A}^2\text{s}$
		t = 8.3ms		84.4	$\text{A}^2\text{s}$
		t = 10ms	Sinusoidal Half Wave, No Voltage Reapplied, Initial $T_J = +125^\circ\text{C}$	131.0	$\text{A}^2\text{s}$
		t = 8.3ms		119.3	$\text{A}^2\text{s}$
Maximum $I^2\sqrt{t}$	$I^2\sqrt{t}$	t = 0.1 to 10ms, no voltage reapplied		1310	$\text{A}^2\sqrt{\text{t}}$
Threshold Voltage, Low level	$V_{T(TO)1}$	$T_J = +125^\circ\text{C}$ , $(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$		0.88	V
Threshold Voltage, High level	$V_{T(TO)2}$	$T_J = +125^\circ\text{C}$ , $(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$		1.12	V
On-State Slope Resistance, Low Level	$r_{t1}$	$T_J = +125^\circ\text{C}$ , $(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$		1.20	$\text{m}\Omega$
On-State Slope Resistance, High Level	$r_{t2}$	$T_J = +125^\circ\text{C}$ , $(\pi \times I_{T(AV)} < I < 20 \times \pi \times I_{T(AV)})$		0.86	$\text{m}\Omega$
Maximum On-State Voltage Drop	$V_{TM}$	$T_J = +125^\circ\text{C}$ , $I_{TM} = \pi \times I_{T(AV)}$ , $180^\circ$ Condition, Av. Power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$		1.5	V
Maximum Holding Current	$I_H$	Anode Supply = 12V, Initial $I_T = 30\text{A}$ , $T_J = +25^\circ\text{C}$		500	mA
Maximum Latching Current	$I_L$	Anode Supply = 12V, Resistive Load = $1\Omega$ , Gat Pulse: 10V, 100 $\mu\text{s}$ , $T_J = +25^\circ\text{C}$		300	mA
Maximum Peak Gate Power	$P_{GM}$	$T_J = +125^\circ\text{C}$ , $t_p \leq 5\text{ms}$		10	W
Maximum Average Gate Power	$P_{G(AV)}$	$T_J = +125^\circ\text{C}$ , f = 50Hz		2.0	W
Maximum Peak Gate Current	$+I_{GM}$	$T_J = +125^\circ\text{C}$ , $t_p \leq 5\text{ms}$		3.0	A
Maximum Peak Negative Gate Voltage	$-V_{GT}$	$T_J = +125^\circ\text{C}$ , $t_p \leq 5\text{ms}$		5.0	V
Maximum Required DC Gate Trigger Voltage to Trigger	$V_{GT}$	$T_J = -40^\circ\text{C}$	Anode Supply = 12V, Resistive Load: $R_A = 1\Omega$	4.0	V
		$T_J = +25^\circ\text{C}$		3.0	V
		$T_J = +125^\circ\text{C}$		2.0	V
Maximum Required DC Gate Trigger Current to Trigger	$I_{GT}$	$T_J = -40^\circ\text{C}$	Anode Supply = 12V, Resistive Load: $R_A = 1\Omega$	350	mA
		$T_J = +25^\circ\text{C}$		200	mA
		$T_J = +125^\circ\text{C}$		100	mA
Maximum Gate Voltage that will not Trigger	$V_{GD}$	$T_J = +125^\circ\text{C}$ , Rated $V_{DRM}$ Applied		0.3	V
Maximum Gate Current that will not Trigger	$I_{GD}$	$T_J = +125^\circ\text{C}$ , Rated $V_{DRM}$ Applied		10	mA
Maximum Rate of Rise of Turned-On Current	di/dt	$T_J = +125^\circ\text{C}$ , $I_{TM} = 400\text{A}$ , Rated $V_{DRM}$ Applied		500	$\text{A}/\mu\text{s}$
Typical Delay Time	$t_d$	$T_J = +25^\circ\text{C}$ , Gate Current = 1A $di_G/dt = 1\text{A}/\mu\text{s}$ , $V_D = 0.67\% V_{DRM}$		1.0	$\mu\text{s}$
Typical Rise Time	$t_r$			2.0	$\mu\text{s}$
Typical Turn-Off Time	$t_q$	$T_J = +25^\circ\text{C}$ , $I_{TM} = 300\text{A}$ , $-di/dt = 15\text{A}/\mu\text{s}$ , $V_R = 50\text{V}$ , $dV/dt = 20\text{V}/\mu\text{s}$ , Gate 0V, 100 $\Omega$		50-150	$\mu\text{s}$

### Circuit Diagram



**NOTE:** Can be used with Heat Sink NTE441A